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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,289	12/28/2001	Young-Hun Ha	8733.560.00	2930

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EXAMINER	
DI GRAZIO, JEANNE A	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,289	HA ET AL.	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *9 and 12-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Priority to Korean Patent Application No. 2000-85421 (Dec. 29, 2000) is claimed.

Election/Restrictions

Applicant's election with traverse of Species A (claims 1-8 and 10-11 readable thereon) in the reply filed on May 21, 2004 is acknowledged. The traversal is on the ground(s) that claims 9 and 18-20 (Species B) are not a species distinct from the invention of the elected claims.

This is not found persuasive because with respect to claim 9, Applicant defines a seal pattern forming region between a display area and a non-display area of a lower substrate and a passivation layer is removed in the seal pattern forming region. However, claim 1 defines the seal pattern as formed in a boundary region between the display area and the non-display area. These appear to be different species of the claimed invention. With regard to claim 18, the method steps include a spacer-dispensing step and seal pattern forming process performed on one of only one substrate or on both upper and lower substrates, respectively, wherein such step does not appear in Applicant's other claimed method steps.

The requirement is still deemed proper and is therefore made **FINAL**.

Claim Objections

Claim 2 is objected to because of the following informalities. As to claim 2, the limitation "wherein the lower substrate further includes a first substrate, the display area and the non-display area" is unnecessarily confusing. This limitation is confusing because Applicant's relevant Figure 6 illustrates the lower transparent substrate (110) and transparent substrate (1) upon which the active elements are formed as one unified single substrate. The Examiner interprets the above noted limitation consistent with Applicant's Figure 6 and thus the lower substrate of the applied prior art is presumed to meet this limitation as one unified single substrate.

Appropriate correction is **required**.

Claim 4 is objected to because of the following informalities. As to claim 4, the limitation "wherein the upper substrate includes a second substrate" is unnecessarily confusing. This limitation is confusing because Applicant's relevant Figure 6 illustrates the upper transparent substrate (120) and transparent substrate (also designated as "1") upon which the color filter and common electrode elements are formed as one unified single substrate. The Examiner interprets the above noted limitation consistent with Applicant's Figure 6 and thus the upper substrate of the applied prior art is presumed to meet this limitation as one unified single substrate.

Appropriate correction is **required**.

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent 6,552,764 B2 (to Fujioka et al.)(filed: July 21, 1999).

As to claim 1, Fujioka discloses, with reference to Figure 13, a lower substrate (101A, active matrix substrate) including a seal pattern forming region (103) between a display area and a non-display area of the lower substrate (101A), an interlayer insulation film (Applicant's "passivation layer")(104) removed in the seal region (103)(non-display region), an upper substrate (color filter substrate 102A), a seal pattern formed in a boundary region between the display area and the non-display area of the lower substrate (101A) and a liquid crystal layer (111) between the upper (102A) and lower (101A) substrates (See also Figure 1)(Figure 1 is a plan view illustrating a liquid crystal display element according to each example of the Fujioka invention)(illustrating the seal forming regions and seal patterns between display and non-display areas).

As to claim 2, Fujioka features the lower substrate (101) as having an insulative substrate (101A).

As to claim 3, the lower substrate (101 / 101A) further includes a gate electrode (203a), a gate insulation film (107), a thin film transistor (201), a pixel electrode (202) connected to the thin film transistor (201) on the gate insulating layer (107) and an insulation film (104) on the

thin film transistor (201)(See also Figure 2A and Example 1)(Figure 2A is a cross-section of Figure 1 applicable to all examples of the invention).

As to claim 4, the color filter substrate includes an insulative substrate (102 / 102A) and has a color filter (106 ...) and counter electrode (209).

As to claim 6, Fujioka further has spacers (116).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,552,764 B2 (to Fujioka et al.) in view of United States Patent 6,336,331 B1 (to Sakamoto et al.).

As to claim 5, Fujioka does not appear to explicitly specify that the passivation layer is removed during a photolithographic mask step for simultaneous patterning of an active layer and the passivation layer.

Sakamoto teaches and discloses an active matrix liquid crystal display device having improved terminal connections in which an organic film and passivation film are patterned simultaneously (Column 3, Lines 50-55). Such simultaneous patterning results in a good contact between a terminal and a TAB in an active matrix substrate (Id.) and results in improved yield and efficiency as a result of fewer mask steps needed to pattern the organic film and passivation film separately.

Sakamoto is evidence that ordinary workers in the field of liquid crystal would have found the reason, suggestion, and motivation to simultaneously pattern an organic film and passivation film for good contact between a terminal and a TAB in an active matrix substrate (Id.) and for improved yield and efficiency as a result of fewer mask steps needed to pattern the organic film and passivation film separately.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystal at the time the invention was made to modify Fujioka in view of Sakamoto for good contact between a terminal and a TAB in an active matrix substrate (Id.) and for improved yield and efficiency as a result of fewer mask steps needed to pattern the organic film and passivation film separately.

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,552,764 B2 (to Fujioka et al.) in view of United States Patent 6,400,439 B1 (to Fujioka et al.).

As to claim 7, Fujioka (764 B2) teaches and discloses with reference to Figure 13, forming a lower substrate (101 / 101A) wherein an interlayer insulation film (104) is removed from a seal region (103), forming an upper substrate (102 / 102A) including a second substrate (102 / 102A), a color filter (106), and a counter electrode (209), forming spacers (116) in the display area (Figure 9) between upper and lower substrates (101 / 101A ; 102 / 102A), forming a seal pattern (Figure 1)(seal 103) in the boundary region between the display area and the non-display area of the lower substrate (101 / 101A), assembling upper (102 / 102A) and lower substrate (101 / 101A)(completed device Figure 13, for example), and injecting liquid crystal into an interior of the seal pattern (Column 2, Lines 9-13).

Fujioka (764 B2) does not appear to explicitly specify that the seal pattern contacts a gate insulating layer.

Fujioka (439 B1) teaches and discloses a liquid crystal display device wherein a sealing material directly contacts a gate insulating film through an adhesion reinforcing portion so that the substrates are adhered together with adequate adhesive strength (Column 18, Lines 38-59).

Fujioka (439 B1) is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion, and motivation to have a seal contact a gate insulating layer so that substrates can be adequately adhered together.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Fujioka (764 B2) in view of Fujioka (439 B1) so that substrates can be adequately adhered together.

As to claim 8, Fujioka (764 B2) Figure 2A has forming a gate electrode (203a) on a first substrate (101 / 101A), forming a gate insulating layer (107) on the first substrate (101 / 101A) and on the gate electrode (203a), forming a thin film transistor (201) on the gate insulating layer (107), and forming a pixel electrode (202) on the gate insulating layer (107), the pixel electrode being connected to the thin film transistor (Column 8, Lines 64-67).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,552,764 B2 (to Fujioka et al.).

As to claim 10, Fujioka teaches and discloses a lower substrate (Figure 1, substrate 101) having a display area and a non-display area, an upper substrate (102) having an area corresponding to the display area, the upper substrate (102) and the lower substrate (101) spaced apart and facing each other (Figure 13), a seal pattern (103) formed between the upper (102) substrate and the lower (101) substrate along a boundary region between the display area and the non-display area and a interlayer insulation film (107) removed from the seal region (103).

Fujioka teaches that prior art liquid crystal display elements have a sealing material with an injection hole into which is injected liquid crystal and then the injection hole is closed with a UV setting resin and the seal having spacers therein serves to define a gap between substrates and to attach the substrates together (Background of the Invention, Column 2, Lines 1-13).

Fujioka is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion, and motivation to have a sealing material with an injection hole into

which is injected liquid crystal and then the injection hole is closed with a UV setting resin and the seal having spacers therein serves to define a gap between substrates and to attach the substrates together (Background of the Invention, Column 2, Lines 1-13).

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to combine the embodiments of Fujioka with the prior art teachings of Fujioka to arrive at a sealing material with an injection hole into which is injected liquid crystal and then the injection hole is closed with a UV setting resin and the seal having spacers therein serves to define a gap between substrates and to attach the substrates together (Background of the Invention, Column 2, Lines 1-13).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 6,552,764 B2 (to Fujioka et al.) in view of Japanese Patent Application 02-220032 (to Obara et al.).

As to claim 11, Fujioka does not appear to explicitly specify that the seal pattern is formed by a screen-printing process using thermosetting resin that includes glass fiber.

Obara teaches and discloses an electro-optic device wherein a thermosetting epoxy resin is used as a seal, the thermosetting epoxy resin is made by screen-printing and contains glass fiber spacers for seal strength and uniformity (Abstracts).

Obara is evidence that ordinary workers in the field of liquid crystals would have found the reason, suggestion, and motivation to form a thermosetting seal with glass fibers by screen printing for seal strength and uniformity.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Fujioka in view of Obara for seal strength and uniformity.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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PRIMARY EXAMINER